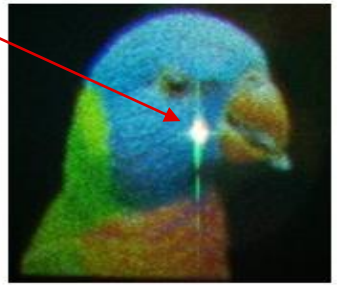
Methods for Removing/Reducing 0th Order Energy Artifacts in PLM Systems

3 Fundamental Approaches

Maximizing the hologram brightness (steering efficiency) means keeping the steered light as centered in the image (far-field envelope/sinc-function) as possible. The remaining flat state light (0^{th} order) is also centered in this region and can be problematic even though the absolute amount of energy is quite low (generally <1%). There are 3 fundamental approaches to removing the artifact:

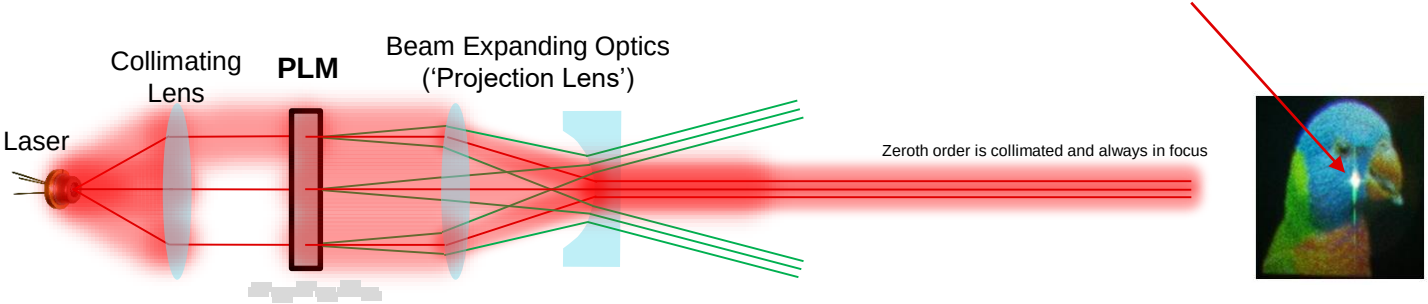
1. Block or mask the spot
2. Expand the spot
3. Tile image away from the spot and recombine



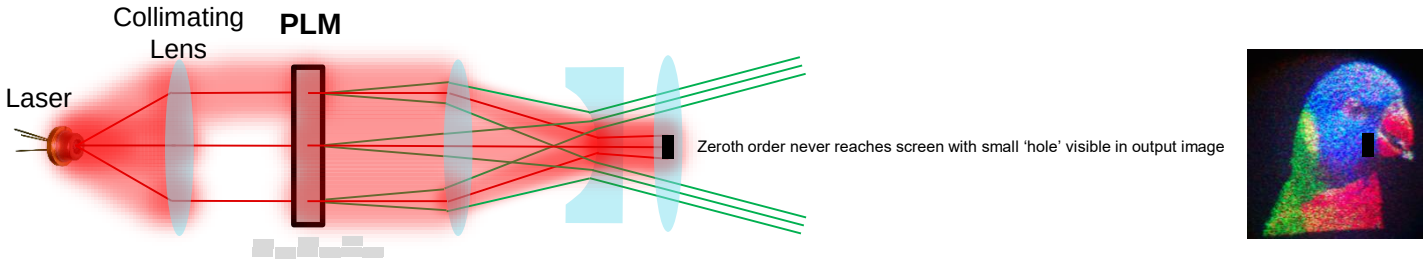
Blocking/Masking the Spot

PLM image rays
Zeroth order rays

Far-field Fourier plane produces a focused PLM image and focused zeroth order (flat-state) beam



Adding a physical mask (i.e. printed on a glass slide) in the projection optics stops the energy from reaching the screen.

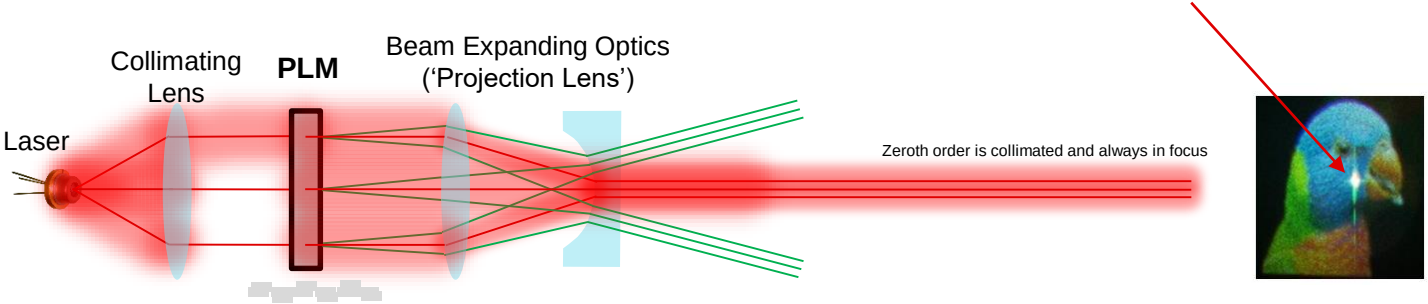


**Good for small Etendue lasers where PSF represent a small portion of the image*

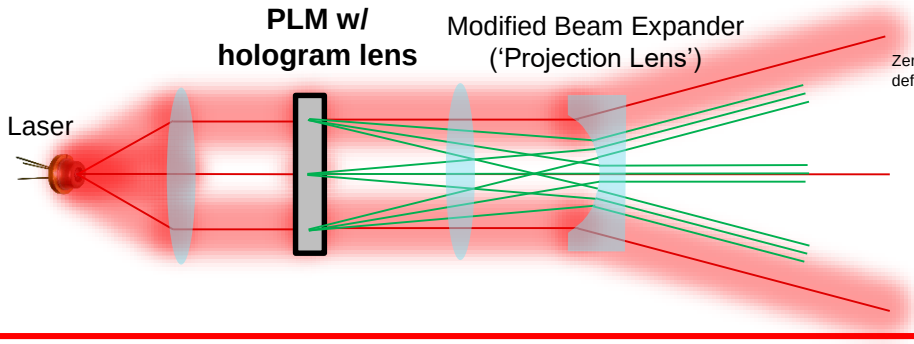
Expanding the Spot

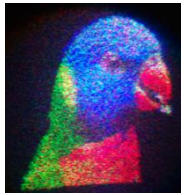
PLM image rays
Zeroth order rays

Far-field Fourier plane produces a focused PLM image and focused zeroth order (flat-state) beam



Adding a spherical wave phase delay to the phase function ('hologram lens') paired with a modified projection lens recreates a new Fourier plane where the PLM image is focused while projection lens defocuses the zeroth order beam

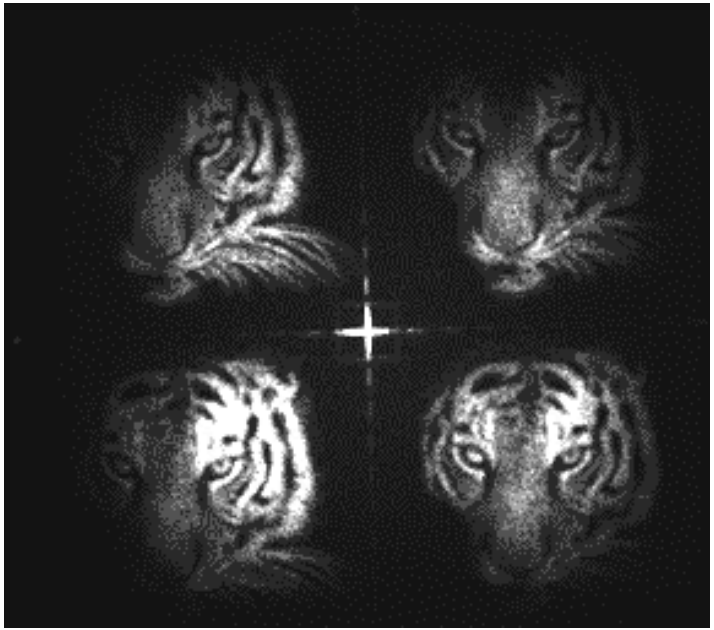




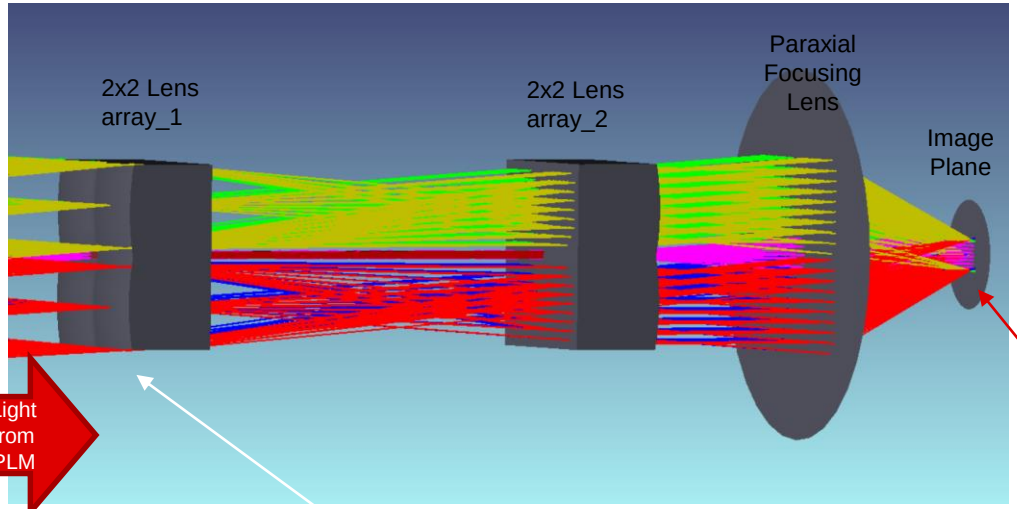
Beam expander must be designed with simulated hologram lens

Tile and Recombine

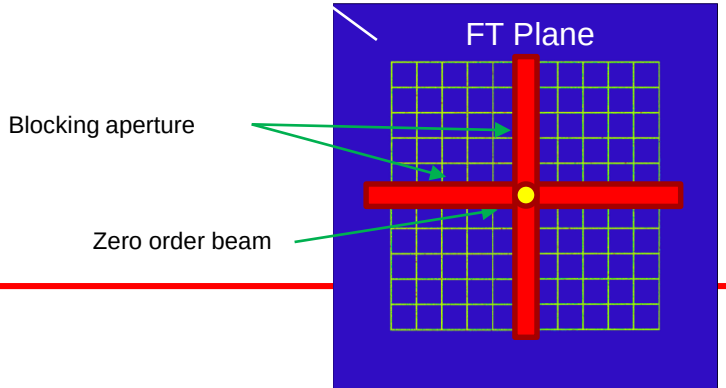
The native 4 images created nearest the 0^{th} order can be recombined while blocking/re-using the flat-state light. This improves efficiency and uniformity while eliminating the undesired artifact.

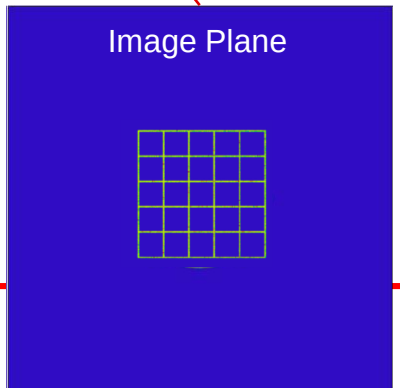


Blocking Technique

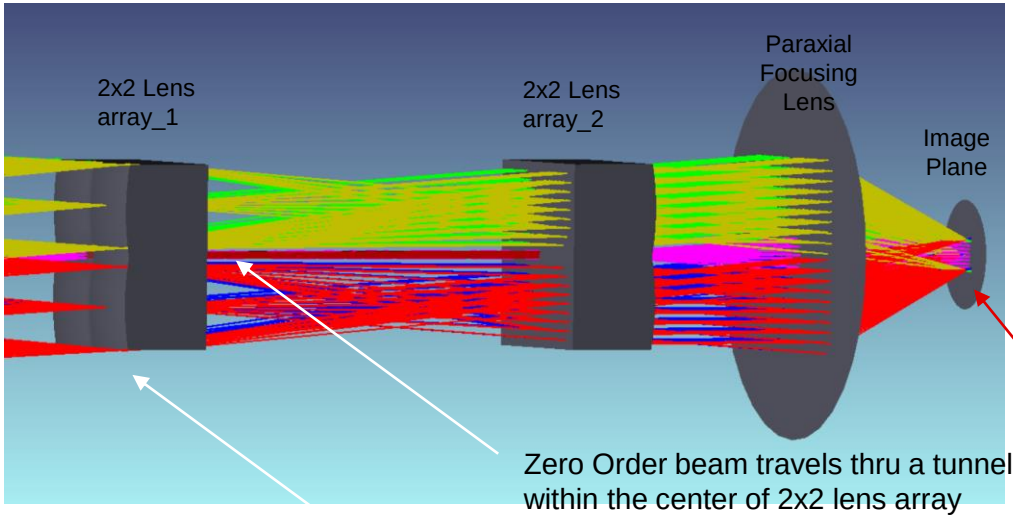


- One method blocks zero order light at the Fourier Transform plane of the optical system
- Image and contrast are high but all of the zero order light is lost

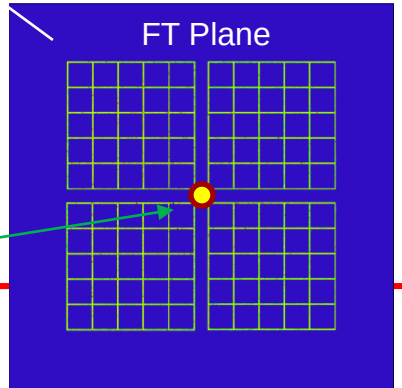


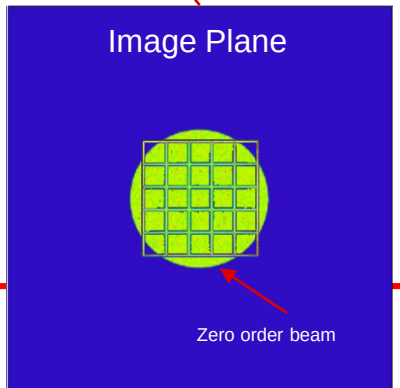


Blocking Technique



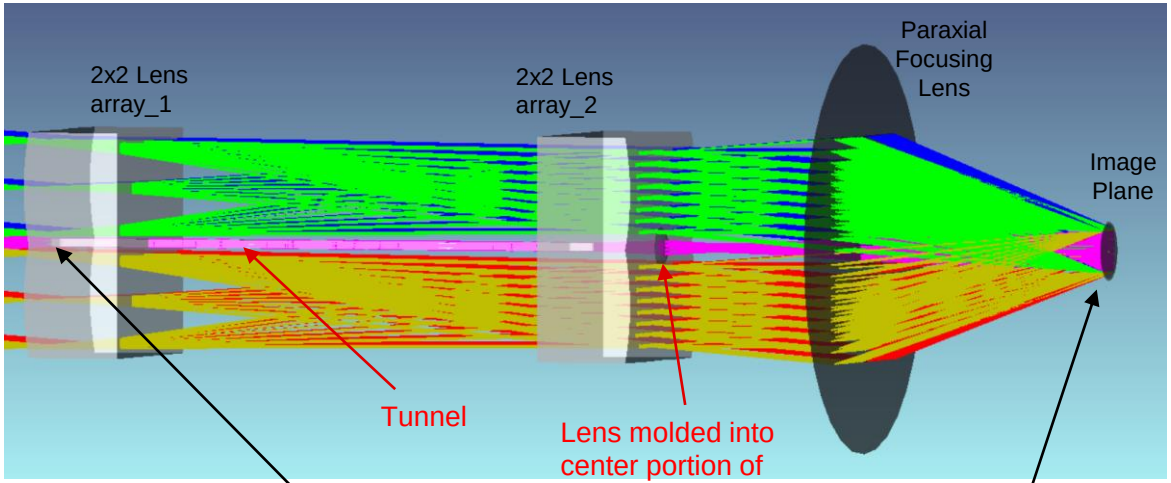
- One method to mitigate the loss of zero order is to use allow the zero order to defocus and spread over the SLM
- Some light is recaptured but achieving zero order illumination beam uniformity is unlikely

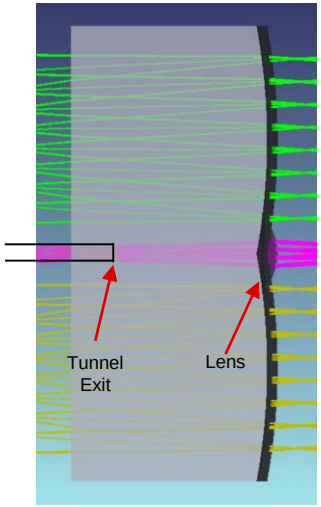




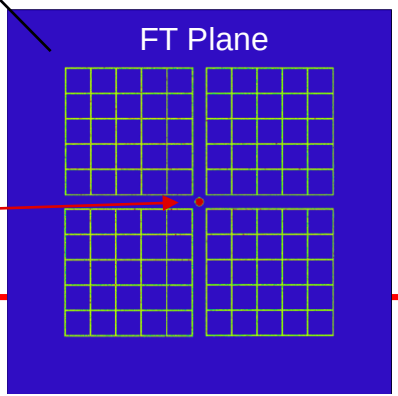
* Note: defocused zero order light is shown as uniform but it is likely to be significantly nonuniform depending on the illumination source

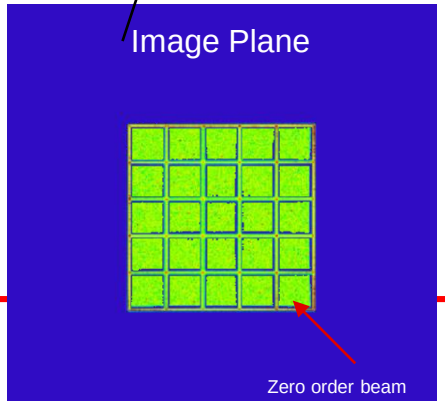
Expanding Technique





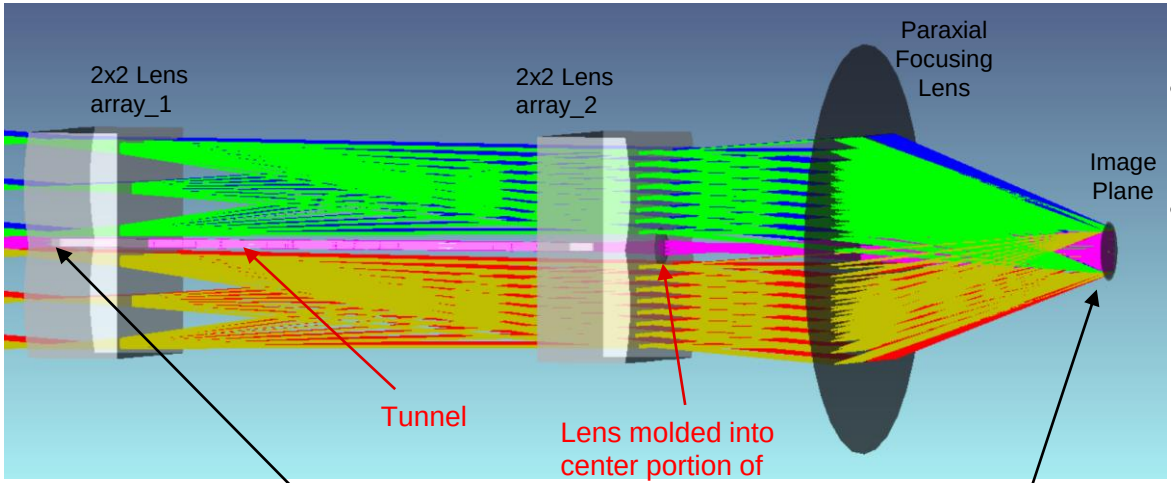
The lens molded into the lens array allows the zero order light to be spread out and match the PLM image size. It is now rectangular compared to circular thus improving efficiency. The focal length for the zero order beam lens is different than the other 2x2 cells.



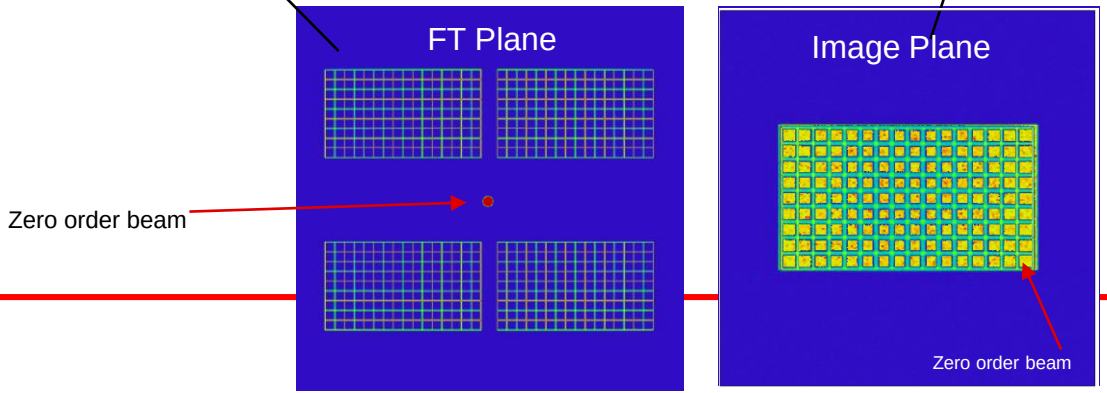


Note: Lens array_2 is a different part than lens array_1 due to the added molded curve for the zero order beam

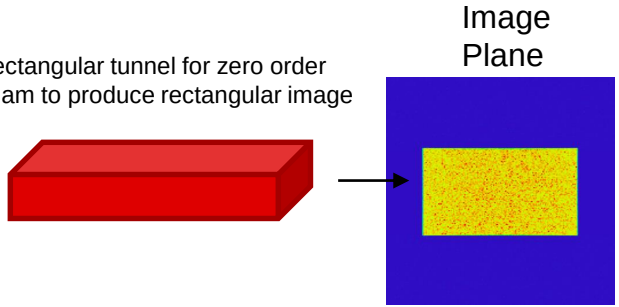
Expanding Technique



- Tunnel aspect ratio can adjust to fit the aspect ratio of the image
- Minimizes overfill, maximizes illumination uniformity and maximizes efficiency of PLM illumination



Rectangular tunnel for zero order beam to produce rectangular image



Tuning PLM Mirror Bias

Mirror Bias Introduction

- The PLM can be tuned to any wavelength in the visible spectrum (405nm to 650nm).
- This tuning is achieved through the parameter Mirror Bias, and it dictates the displacement of the highest bit state.
  - The Mirror Bias voltage is applied globally to all mirrors in the array.
- A mirror's displacement is therefore determined by the electrostatic forces between the mirror (mirror bias) and the electrodes (memory cell configuration or 'state').
  - Larger displacements require higher electrostatic forces between the mirror and electrodes, and thus lower Mirror Bias values.
- States are separated approximately by the normalized deflection table provided for each specific PLM device as mirror bias is tuned. The absolute physical state displacements will change with applied Mirror Bias.

Mirror Bias and Electrode Voltages

- The difference between the Voffset (electrode) voltage and the Mirror Bias voltage determines the maximum displacement of the PLM mirrors.
- The EVM provides a connector on the PLM board to input the Mirror Bias voltage
- The EVM generates the Voffset (electrode) voltage on board but it can also be supplied externally.
- Mirror Bias is used to adjust the mirror displacement for different wavelength applications
  - Proposed method for mirror bias optimization is found on the next slide
- Specifications for Mirror Bias and Voffset are in the table below.
- Until tuned, start with the Mirror Bias at a relatively high voltage like 4V. This avoids overdriving the mirrors
- **Power Sequencing: Power On: Mirror Bias followed by 12V. Power Off: 12V followed by Mirror Bias**

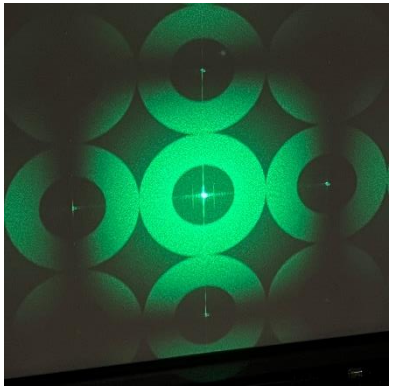
PARAMETER	MIN	NOM	MAX	UNIT
Mirror Bias Supply				
Voltage	0		5	V
Current			10	mA
Voffset				
Voltage		10		V
Current			100	mA

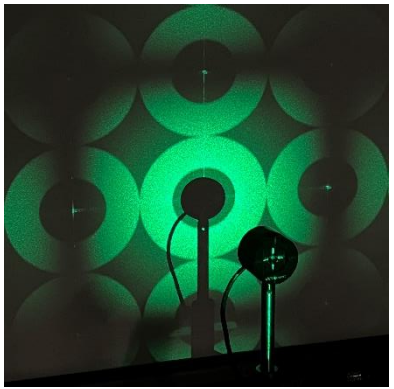
Tuning Mirror Bias

- It is important to identify the optimal Mirror Bias for each device and wavelength.
- There are multiple methods to tune the Mirror Bias. We have found that distribution of states is pretty similar for most holograms generated with the GS algorithm, so we recommend the tuning procedure below.

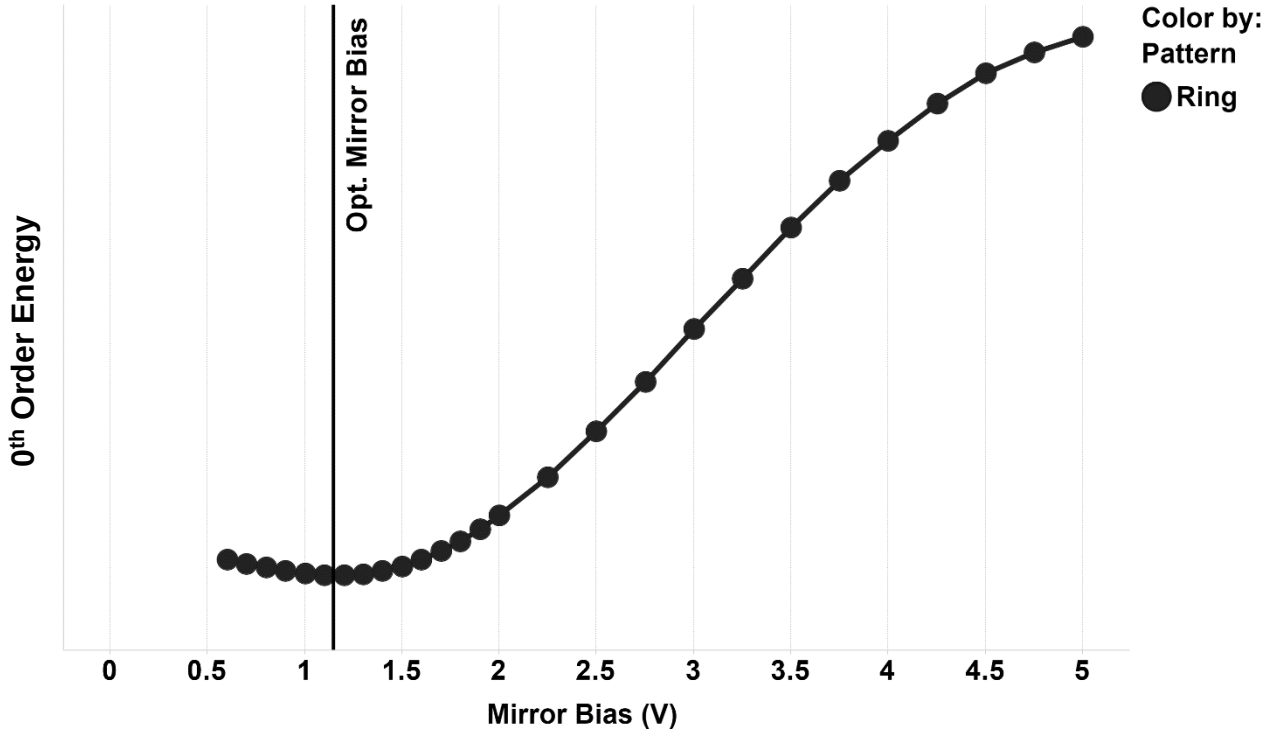
Recommend Mirror Bias Tuning Procedure:

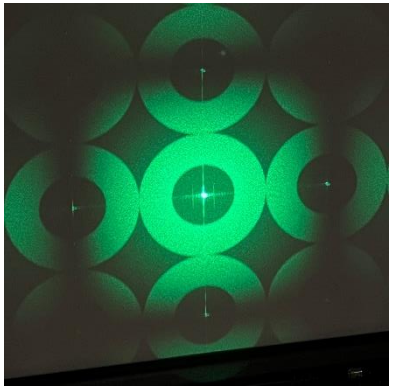
1. Start with the Mirror Bias at a relatively high voltage like 4V.
2. Open the hologram CGH_Ring.bmp provided for the given PLM device.
   - You should see a series of rings centered on the native diffraction orders.
3. Place a photodiode detector onto the 0th diffraction order to record the energy present in the order.
   - When the Mirror Bias is optimized, this 0th order energy will be minimized.
4. Slowly reduce the Mirror Bias voltage until the 0th order energy is minimized. This voltage will be the optimal Mirror Bias voltage for that wavelength.
   - Avoid going too far past the optimal Mirror Bias voltage (too low), especially for longer wavelengths, as you risk landing mirrors that may remain stuck.
   - See the following slide for a graph of this process.

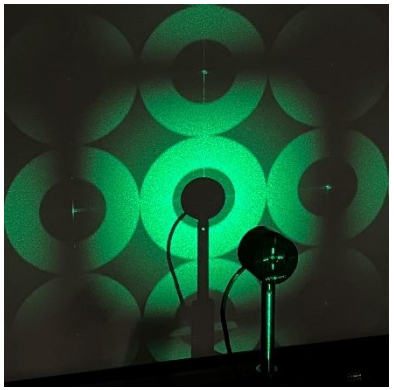




Tuning Mirror Bias







PLM heat load calculation

Determining heat load on PLM

- **Total heat load = absorbed optical load + electrical load**
- **Absorbed optical load, no overfill outside active array mirrors:**

$$\alpha = FF * (1 - MR) + (1 - FF) + 2 * \alpha_{bulk\ window}$$

Absorption in mirror

Absorption in gaps (100%)

Absorption in bulk window (wavelength, window material and thickness dependent) 2 passes

FF = fill factor of mirror array (10.8 um pixel, 0.3 um gaps = 0.945 fill factor)

MR = mirror reflectivity (wavelength dependent, 94% @1064 nm)

$\alpha_{bulk\ window}$ = bulk window absorption per pass (Eagle XG @ 1.05 mm thick, 24 degree AOI, 1064 nm = 0.007)

- **Absorbed optical load = Q_incident * α**

Determining heat load on PLM (example)

- 10.8 um SHV device with 100W incident power @1064 nm
  - FF = 0.945
  - MR = 0.94
  - $\alpha_{bulk\ window}$ = 0.007 per pass

$$\alpha = FF * (1 - MR) + (1 - FF) + 2 * \alpha_{bulk\ window}$$

$$\alpha = 0.945 * (1 - 0.94) + (1 - 0.945) + 2 * 0.007$$

$$\alpha = 0.1257$$

- Absorbed optical load = 100W * 0.1257 = 12.57W

Determining mirror temperature rise above silicon

- For very high power applications, the temperature rise of the mirror above the silicon die is significant

$$Delta\_T_{MIRROR-TO-SILICON} = Q_{MIRROR} * R_{MIRROR-TO-SILICON}$$
$$Q_{MIRROR} = Q_{INCIDENT\_MIRROR} * [FF * (1 - MR)]$$

Q_{MIRROR} = absorbed heat load on a single mirror

$Q_{INCIDENT\_MIRROR}$ = Incident optical power on an individual mirror

$R_{MIRROR-TO-SILICON}$ = Thermal resistance, individual mirror to silicon die

Determining mirror temperature rise above silicon (example)

- 10.8 um SHV with 500W incident (uniform over entire array)
- For very high power applications, the temperature rise of the mirror above the silicon die is significant

$$Delta\_T_{MIRROR-TO-SILICON} = Q_{MIRROR} * R_{MIRROR-TO-SILICON}$$
$$Q_{MIRROR} = Q_{INCIDENT\_MIRROR} * [FF * (1 - MR)]$$

Q_{MIRROR} = absorbed heat load on a single mirror

$Q_{INCIDENT\_MIRROR}$ = Incident optical power on an individual mirror

$R_{MIRROR-TO-SILICON}$ = Thermal resistance, individual mirror to silicon die

$$Q_{MIRROR} = [\frac{500W}{(1920*1080)}] * [0.945 * (1 - 0.94)] = 1.37e\text{-}5\ W$$
$$R_{MIRROR-TO-SILICON}(10.8\ um\ SHV\ pixel) = 7.88e5\ ºC/W$$
$$Delta\_T_{MIRROR-TO-SILICON} = Q_{MIRROR} * R_{MIRROR-TO-SILICON} = 1.37e{-}5\ W * 7.88e5\ ºC/W = 10.8\ ºC$$

Mirror Reflectivity

- **Applications Note DLPA083B - DMD Optical Efficiency for Visible Wavelengths, page 9**

5 Mirror Reflectivity

The active array area consists of a large rectangular array of aluminum based mirrors. The mirrors are nominally 89% reflective in the visible range (420 to 680 nm).

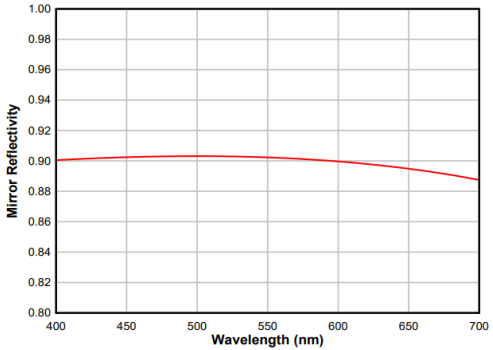


Figure 5-1. DMD Mirror Typical Reflectivity

- **This is for our standard aluminum mirror in the visible range. At 1064 nm, reflectivity is 94%. Reflectivity generally follows reflectivity for polished aluminum vs. wavelength.**
- **Reflectivity with a dielectric coating will be different**

Bulk window absorption

- Applications Note DLPA031E, Wavelength Transmittance Considerations for DLP® DMD Window

- We have measured window transmission for various DLP windows, but not bulk absorption. Measurements on a few samples indicate most of the transmissive loss is reflective rather than absorptive.
  - Type A devices use Corning 7056 glass
  - WLP/hDMD devices use Corning Eagle XG glass

- We plan to measure bulk absorption vs wavelength for other windows such as the 0.9 type A (Corning 7056 glass)
- The example here shows measurements from the DLP650LNIR window (WLP – Corning Eagle XG)