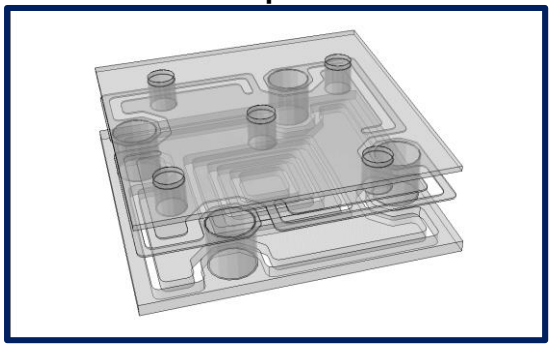
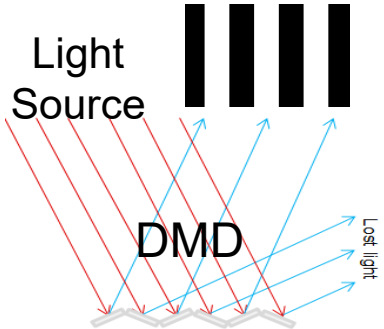
TI DLP® Products:
PLM Informational

Amplitude (DMD) and Phase Light Modulation (PLM)

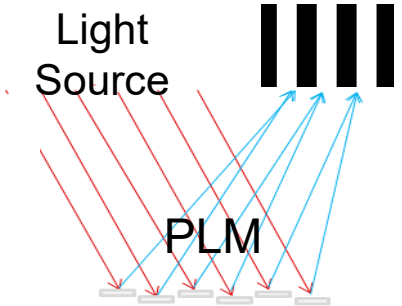
Current Product

Development





Amplitude Modulation

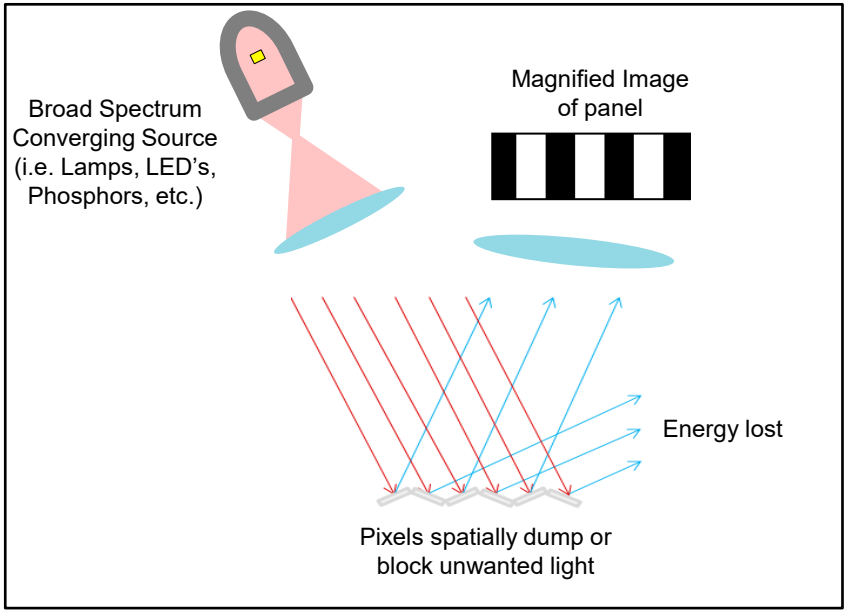


Phase Modulation

Spatial Light Modulation (SLM)

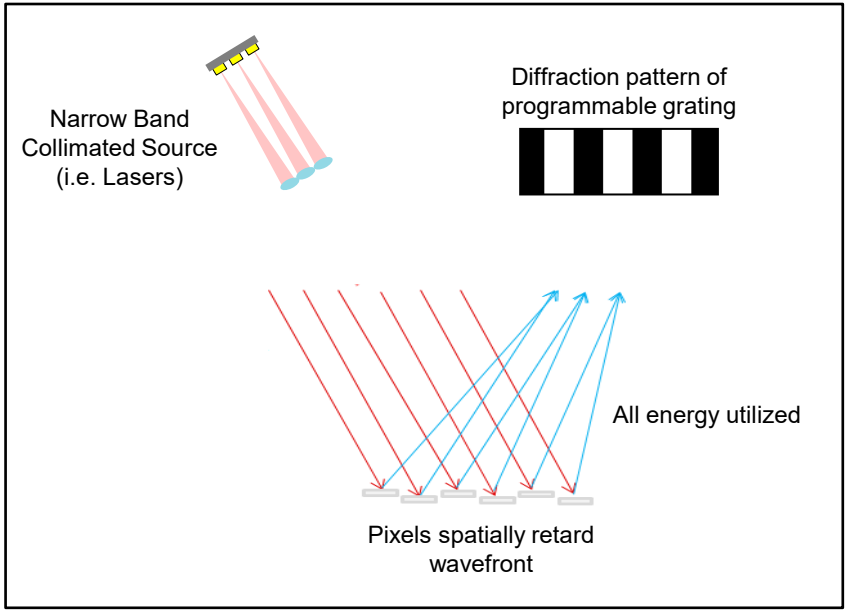
Amplitude (ALM) vs. Phase (PLM) Systems

ALM



Traditional Projection

PLM



Laser Enabled Diffraction System

Technology Advantages

Amplitude (ALM) vs. Phase (PLM) Systems

ALM

- *Resolution (typically)*
- *Wide Light Source Compatibility*
- *Computational Expense*

Traditional Projection

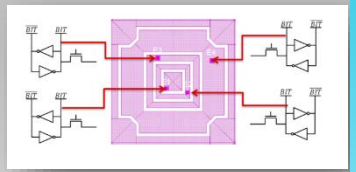
PLM

- *Efficiency*
- *System Size*
- *Peak Lux*

Laser Enabled Diffraction System

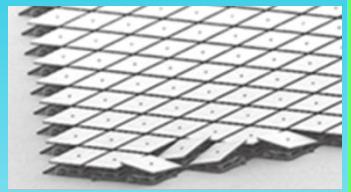
PLM | Technology

CMOS IP



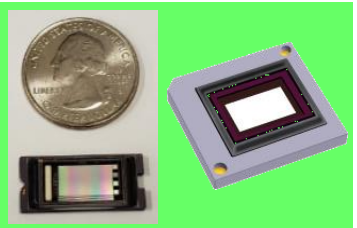
- CMOS Node
  - SRAM with BSA architecture
  - DMD interfaces

Process



- MEMS Process
  - Uses mature DMD process
  - Filled Mirror Via
  - Supports visible

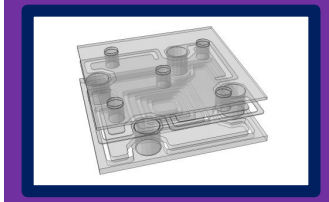
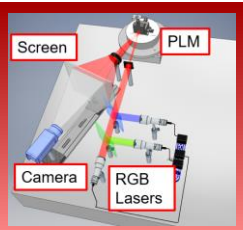
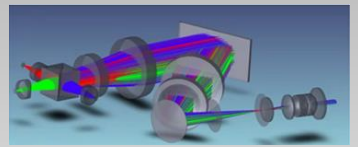
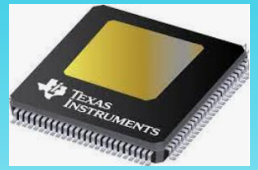
Package



- DMD Packaging
  - Same LGA & PGA packages
  - WLP, hDMD, Type A

DLP DMD tech well suited for PLM Device

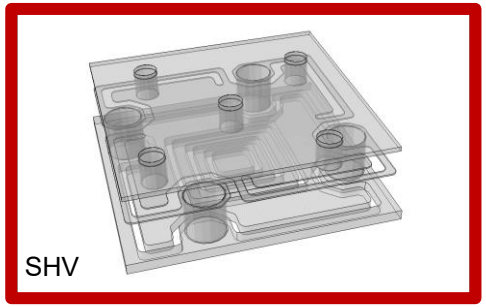
PLM | Technology

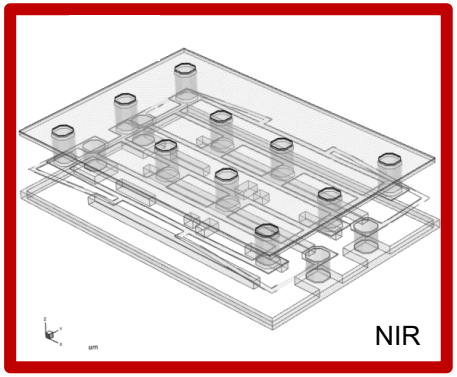
MEMS IP	Test	System – Optics	System – Controller
			
❑ MEMS Design ❑ 4 Hinges ❑ No Contact ❑ Piston Motion	❑ Test Development ❑ H/W ❑ S/W ❑ Parametrics	❑ Optical Design ❑ Illumination ❑ Algorithms ❑ Projection	❑ Controller/FPGA ❑ Translation chip ❑ TI existing chip ❑ New chip

New elements ongoing

Phase Light Modulator Pixel Descriptions

	Visible PLM (SHV)	NIR PLM (TBD)
Pitch	10.8um x 10.8um	16.2um x 10.8um
# States	16	32
State Linearity	0.93	0.98
Fill Factor	94.5%	95.4%
Mirror Reflectivity	89%	95%
Approx. 0th Order Efficiency	70%	85%
Wavelength Support	405nm to 640nm	750nm to 1630nm
Switching Speed	<50us	~50us
Array size	0.67” (1358x800)	0.67” (904x800)
EVM Support	Now	1H25
EVM Frame Rate	1.4kHz	1.4kHz
Samples	Now	1H25
Qualified	2025 (0.98”)	TBD

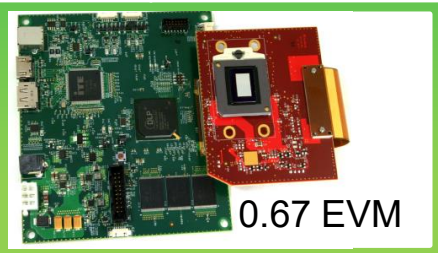




EVM Kits

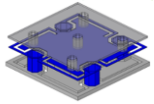
	0.47” PLM EVM	0.67” PLM EVM	0.98” PLM EVM
Interface	HDMI	DisplayPort/HDMI	Serdes[1]
Array Size	960x540	1358x800	2048x1088
Frame Rate	180Hz	Up to1.4kHz[2]	Up to 5kHz
Sync generation	No	Yes	No
λ Control[3]	No	Yes	Yes
Pattern Data/Display	Video Sequenced	Video Sequenced	User controlled

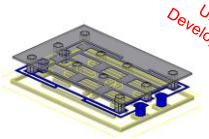
[1] Xilinx Aurora interface.
[2] 720Hz thru HDMI, 1.4kHz thru DisplayPort, 5.6kHz if driven thru stored data (96 frames max).
[3] λ control can also be used for temperature compensation.



- Evaluation Modules
  - Data load
  - Image processing left to the user

Potential Uses for PLM Technology

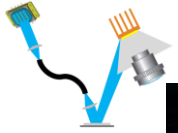


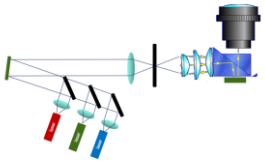


~ Optical Power

3D Print

Headlight





Industrial Lighting

HDR Projection

LiDAR (Outdoor/ Indoor)

Laser Sintering

365 – 405 nm

420 – 700 nm

900 nm – 1550 nm

1550 nm

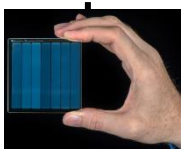
UV

Visible

IR

Digital Ground Projection

Lithography

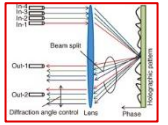


Holographic Data Storage

Heads Up Display

3D Scanning

Optical Switching

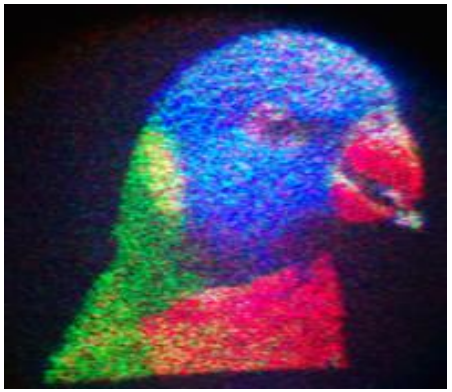


Biomedical Imaging

Questions?

Recommended Literature:

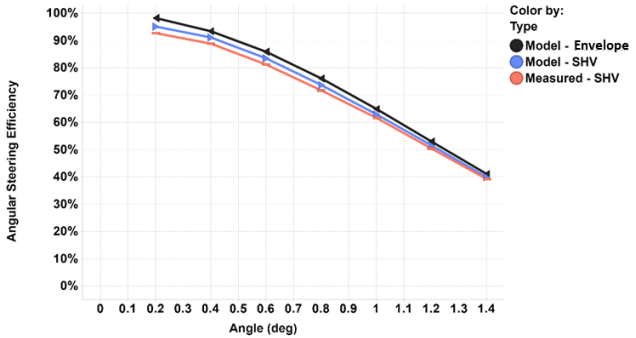
- https://doi.org/10.1117/12.2514483
- https://doi.org/10.1117/12.2550582
- https://doi.org/10.1117/12.2582199
- https://doi.org/10.1117/12.2612227
- http://dx.doi.org/10.1117/12.3003885
- https://www.ti.com/lit/an/dlpa031e/dlpa031e.pdf
- https://www.ti.com/lit/an/dlpa083b/dlpa083b.pdf

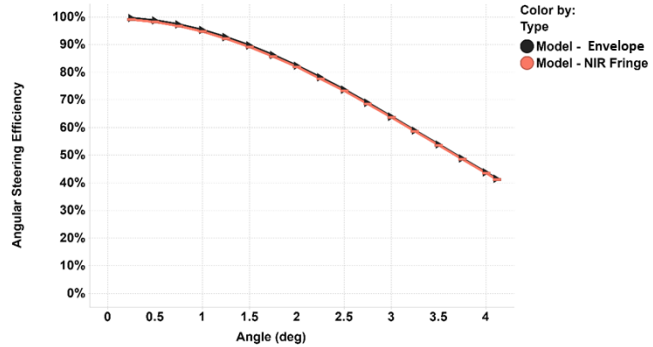


Backup

Efficiency

520 nm, SHV vs Envelope

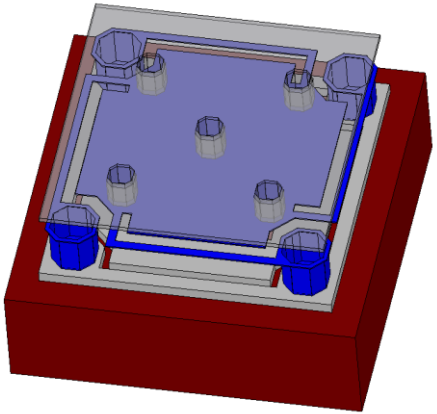


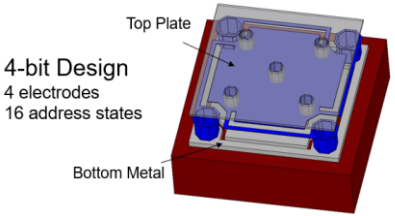


1550 nm, NIR Fringe (10.8 um) vs Envelope

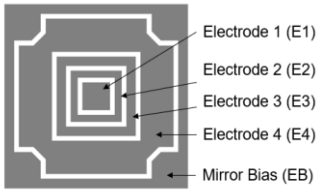
- 0th Order Efficiency (a.k.a. Reflectivity)
  - Fill Factor
  - Mirror Reflectivity
  - Window Transmission
  - Theoretical Max ~77% for SHV
  - Typical > 70% for SHV
- 1st Order Efficiency (a.k.a. Angular Steering Efficiency)
  - Phase Error (quantization, approximations, etc.)
  - Hologram Dependent
  - Theoretical Max = ‘sinc’ Envelope Function
  - Typical > 90% of theoretical (see left) for SHV
- Total Efficiency = 0th Order * 1st Order

PLM device operation

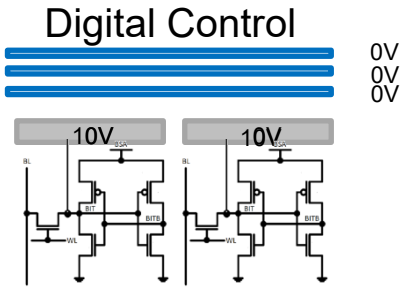




(a) Isometric View

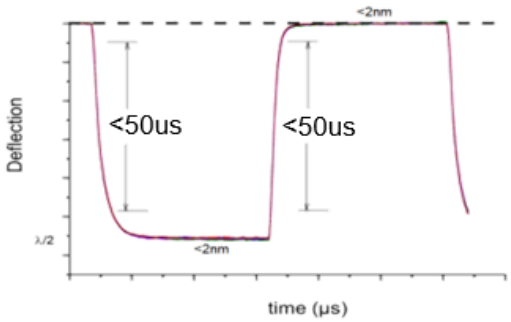


(b) Electrode Design

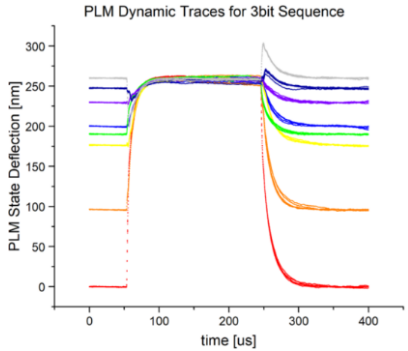


MEMS PLM advantages

- Speed



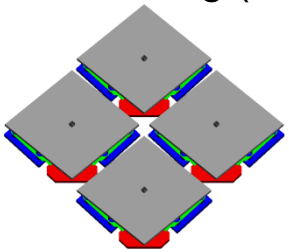
- Static Phase Displacement



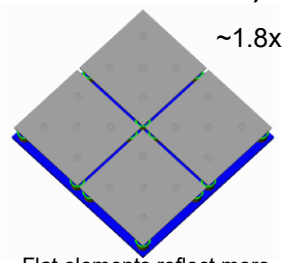
- Operational Range

	Operating Temperature	Storage Temperature
DMD Technology	-40C to 105C (auto)	-40C to 125C
PLM Technology	-40C to 125C (anticipated)	-40C to 125C
Competition	10C to 40C 10C to 70C	-20C to 55C ?

- Power Handling (50W/cm^2 > 3000hr)



Tilted pixels allow light to be absorbed in device



~1.8x DMD

Flat elements reflect more light and allow less to be absorbed in device

PLM Reliability test results

Summary of reliability testing completed to-date

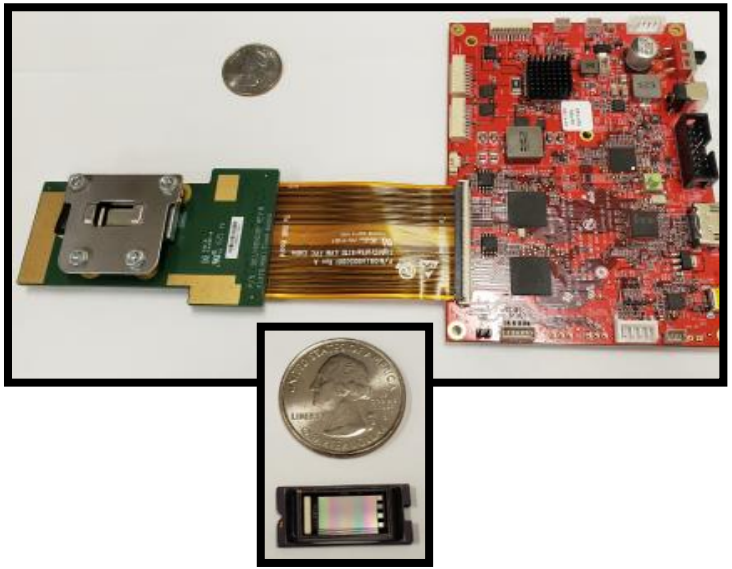
Stress Temperature	Time	Results
-40C	> 1000 hours	No degradation
-20C		
25C		
65C		
95C	> 10000 hours	
125C	> 1000 hours	

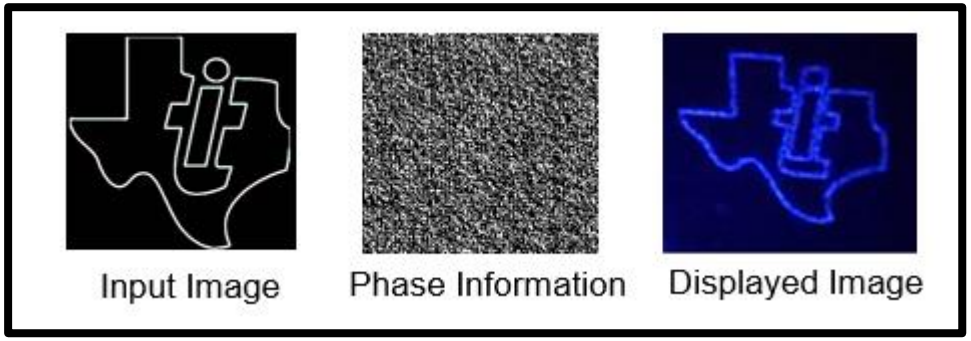
Environmental Test Type	Test Description	Results
Vibration	20 g peak, 20-2000 Hz, 3 axes	No degradation
Mechanical Shock	5 shock pulses, 6 axes, 1500 g peak, 0.5 ms pulse	
Temperature Cycling	2000 cycles, -55C to 125C	
Hot Storage	1008 hours at 125C	
Cold Storage	1008 hours at -40C	

No evidence of degradation due to operation at various temperatures and profiles

Environmentally robust (similar to DMD results)

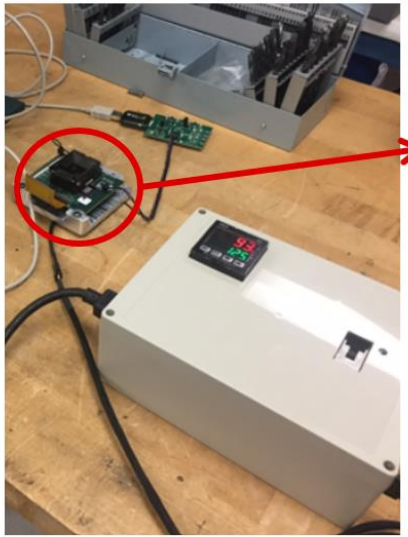
0.47 EVM

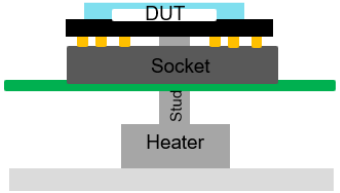


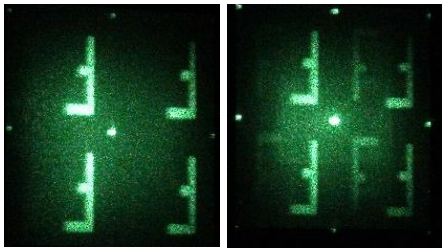


- 0.47 EVM
  - 0.47 device had 960x540 “phixels”
  - Plug and play, just power on, connect HDMI, illuminate with laser
  - Allowed different CGHs on Red, Green, and Blue channels
  - 180Hz display (60Hz HDMI with 3 patterns per frame)
  - Setup for single color use only

0.47 EVM

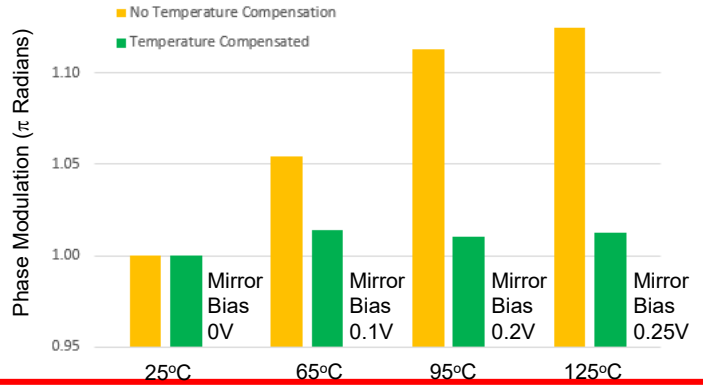






Good display

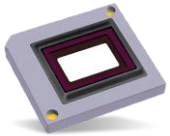
Bad display - conjugate image



What happens at elevated temperatures

- Created a heater stud
- Looked at CGH at screen from 25°C to 95°C
- No Conjugate image seen, so good MEMS actuation
- But we can do better by using temperature compensation thru the MirrorBias pin

0.67 SHV Design Description

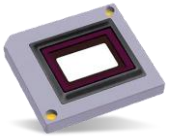


Nominal Displacement Chart

Phase states	Memory (3,2,1,0)	Electrodes (3,2,1,0)	Typical Displacement
0	0011	0000	0%
1	0010	0001	1.07%
2	0001	0010	2.19%
3	0111	0100	4.50%
4	0000	0011	5.98%
5	0110	0101	7.75%
6	0101	0110	12.06%
7	0100	0111	18.50%
8	1011	1000	36.55%
9	1010	1001	39.55%
10	1001	1010	45.10%
11	1000	1011	52.44%
12	1111	1100	63.93%
13	1110	1101	71.16%
14	1101	1110	85.02%
15	1100	1111	100.00%

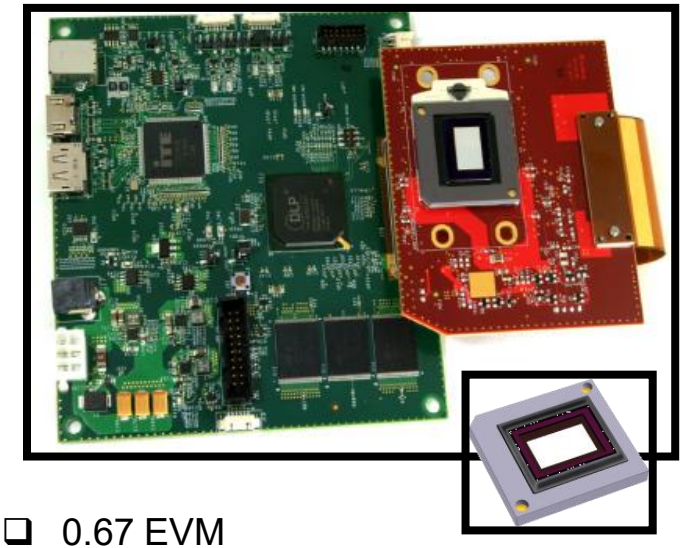
Category	Specification		Units	Recommended	Comments
Array	Pixel Pitch		um	10.8	
	Native Resolution	X	count	1358	
		Y	count	800	
	Array	X	mm	14.67	
		Y	mm	8.64	
	Diagonal		mm	17.02	
	Diagonal		in	0.67	
	Bit-Depth		bits (states)	4 (16)	
	Max Displacement		nm	λ/2 * (15/16)	
	Linearity	>	R^2	0.93	
Electrical	Transition Time (Rise/Fall)	<	us	50/50	10%-90% of Max Displacement
	Load Time	<	us	100	Time to fully load Array
	Frame Rate	>	kHz	6.7	
	Interface			SubLVDS	HDMI/DVI on EVM Reference Design. Dual 442X style controller proposed
	Voffset			10	
	Mirror Bias (MB)	min	V	-0.5	Parts will be bias binned with a nominal voltage given as a function of
	~=3.2-(λ/344.8)+(10-Voffset)	max	V	2.5	wavelength. Final voltage tunning required in system.

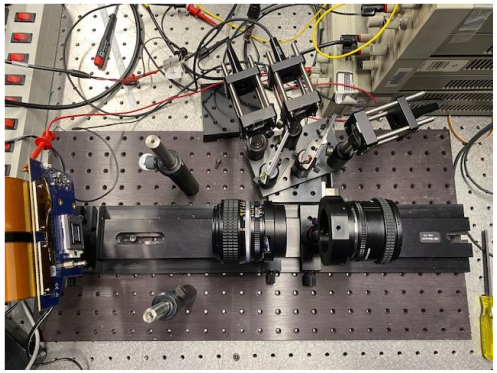
0.67 Performance Description

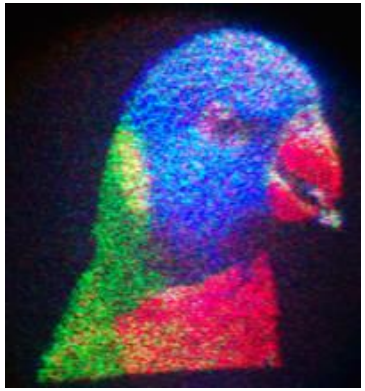


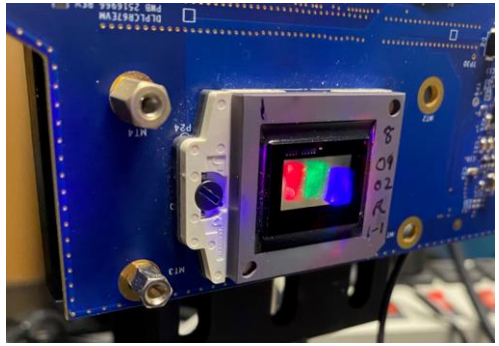
Category	Specification		Units	Recommended	Comments
Optical	0th Order Efficiency	>	%	TBD	0th-order/Incident
	Diffraction Efficiency	>	%	TBD	This is a measure of the energy successfully steered out of the 0th order and is highly depended on hologram. Measurement method under development.
	Diffraction Uniformity	<	%	TBD	This is the max variation of the Diffraction Efficiency across the image field. Measurement method under development.
	Wavelength (λ)	min	nm	436	
		max	nm	650	
	Acceptable Overfill Area	<	%	10	Underfill Recommended
	Incident Illumination Angle	<	deg	20	Angle is measured from normal
	Incident Flux	max	W/cm^2	40	Modeling indicates that this legacy DMD limit is a significant underestimate of this Pixel's capability. Need more testing in this space to find limits.
	Total Power	max	W	51	
Thermal	Storage Temp	min	C	-40	
		max	C	80	
	Operating Temp	min	C	0	
		max	C	90	

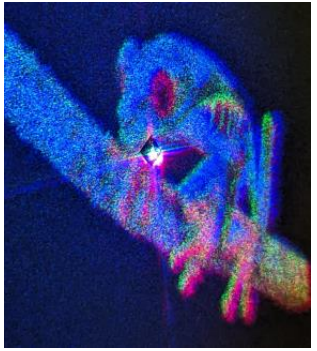
0.67 EVM





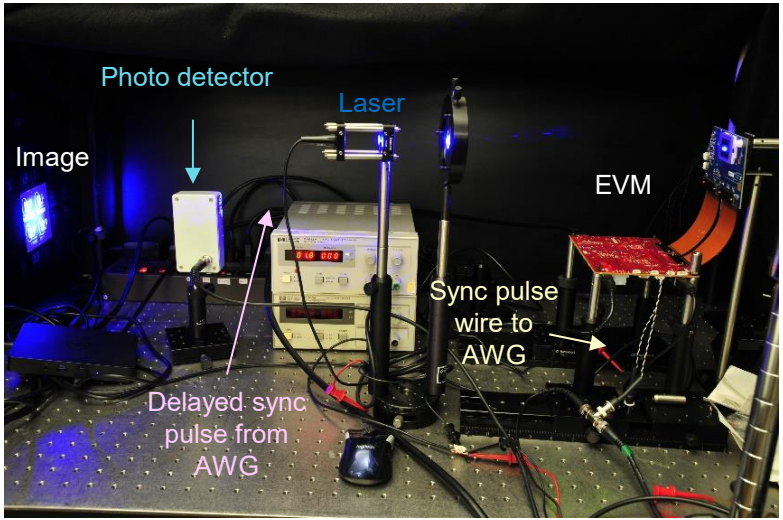


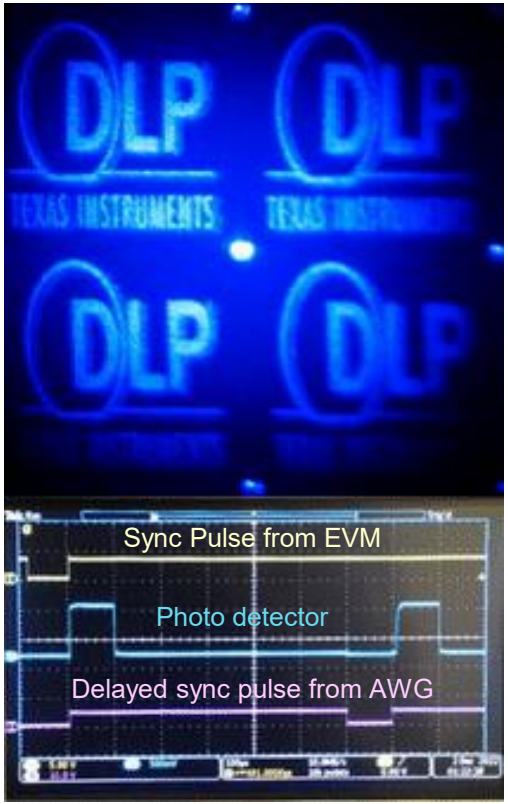




- 0.67 EVM
  - 0.67 device with 1348x800 “phixels”
  - Configurable sync pulses, video input, display time
  - External MirrorBias allows user to set displacement for wavelength and provide temperature compensation
  - 720Hz HDMI, 1.4kHHz DisplayPort, and 5.6kHz burst
  - Available now in limited quantities

0.67 EVM





EVM sync signal generation

- Used to provide sync to AWG
- Laser pulsed to match display pattern
- Delayed pulse of AWG to match PLM data load & switch
  - During data load, “phixels” go to flat state so light goes back to 0th order

DLP Performance Products | 0.98 Design Description

Nominal Displacement Chart

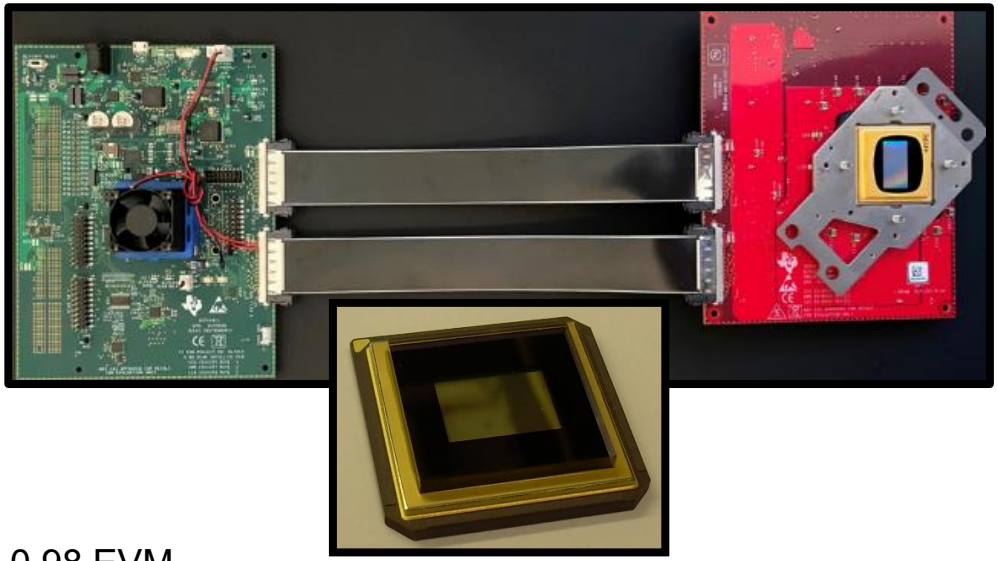
Phase states	Memory (3,2,1,0)	Electrodes (3,2,1,0)	Typical Displacement
0	0011	0000	0%
1	0010	0001	1.07%
2	0001	0010	2.19%
3	0111	0100	4.50%
4	0000	0011	5.98%
5	0110	0101	7.75%
6	0101	0110	12.06%
7	0100	0111	18.50%
8	1011	1000	36.55%
9	1010	1001	39.55%
10	1001	1010	45.10%
11	1000	1011	52.44%
12	1111	1100	63.93%
13	1110	1101	71.16%
14	1101	1110	85.02%
15	1100	1111	100.00%

Category	Specification		Units	Recommended	Comments
Array	Pixel Pitch		um	10.8	
	Native Resolution	X	count	2048	
		Y	count	1088	
	Array	X	mm	22.1184	
		Y	mm	11.7504	
	Diagonal		mm	25.05	
	Diagonal		in	0.99	
	Bit-Depth		bits (states)	4 (16)	
	Max Displacement		nm	λ/2 * (15/16)	
	Linearity	>	R^2	0.93	
Electrical	Transition Time (Rise/Fall)	<	us	50/50	10%-90% of Max Displacement
	Load Time	<	us	100	Time to fully load Array
	Frame Rate	>	kHz	6.7	
	Interface			HSSI	Final integration plan still TBD.
	Voffset			10	
	Mirror Bias (MB)	min	V	-0.5	Parts will be bias binned with a nominal voltage given as a function of wavelength. Final voltage tunning required in system.
	~=3.2-(λ/344.8)+(10-Voffset)	max	V	2.5	

DLP Performance Products | 0.98 Preliminary Performance Desc

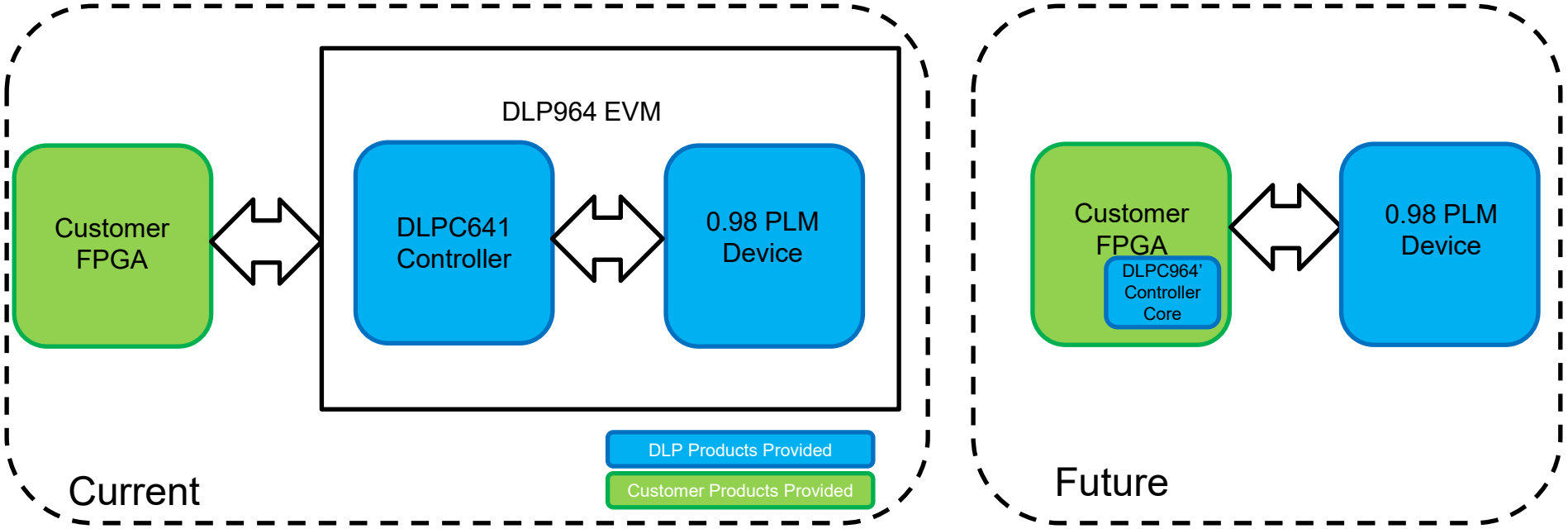
Category	Specification		Units	Recommended	Comments
Optical	0th Order Efficiency	>	%	TBD	0th-order/Incident
	Diffraction Efficiency	>	%	TBD	This is a measure of the energy successfully steered out of the 0th order and is highly depended on hologram. Measurement method under development.
	Diffraction Uniformity	<	%	TBD	This is the max variation of the Diffraction Efficiency across the image field. Measurement method under development.
	Wavelength (λ)	min	nm	436	
		max	nm	650	
	Acceptable Overfill Area	<	%	10	Underfill Recommended
	Incident Illumination Angle	<	deg	20	Angle is measured from normal
	Incident Flux	max	W/cm^2	40	Modeling indicates that this legacy DMD limit is a significant underestimate of this Pixel's capability. Need more testing in this space to find limits.
	Total Power	max	W	104	
Thermal	Storage Temp	min	C	-40	
		max	C	80	
	Operating Temp	min	C	10	
		max	C	65	

0.98 EVM



- 0.98 EVM
  - 0.98 device has 2048x1088 “phixels”
  - User controlled pattern data timing with direct data access thru Xilinx Aurora Interface (LogiCORE™ IP)
  - External MirrorBias allows user to set displacement for wavelength and provide temperature compensation
  - Available first half 2023

0.98 EVM

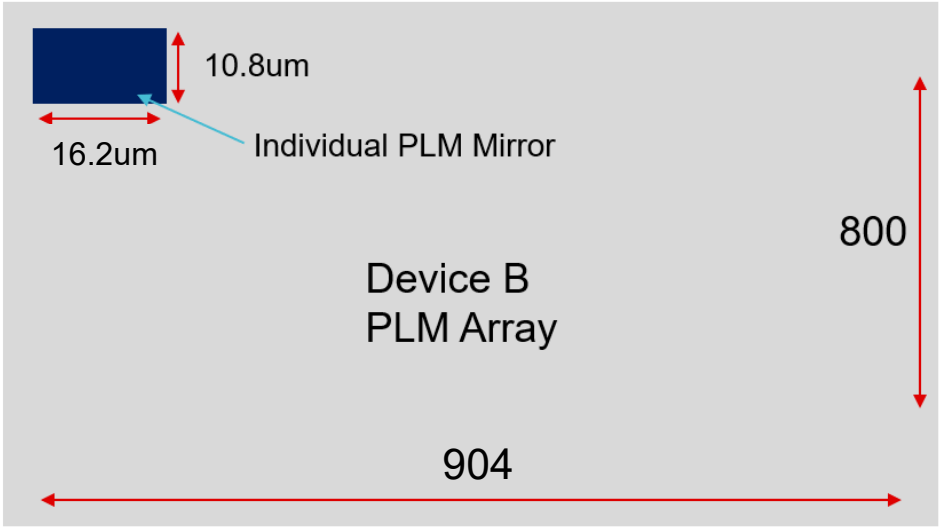


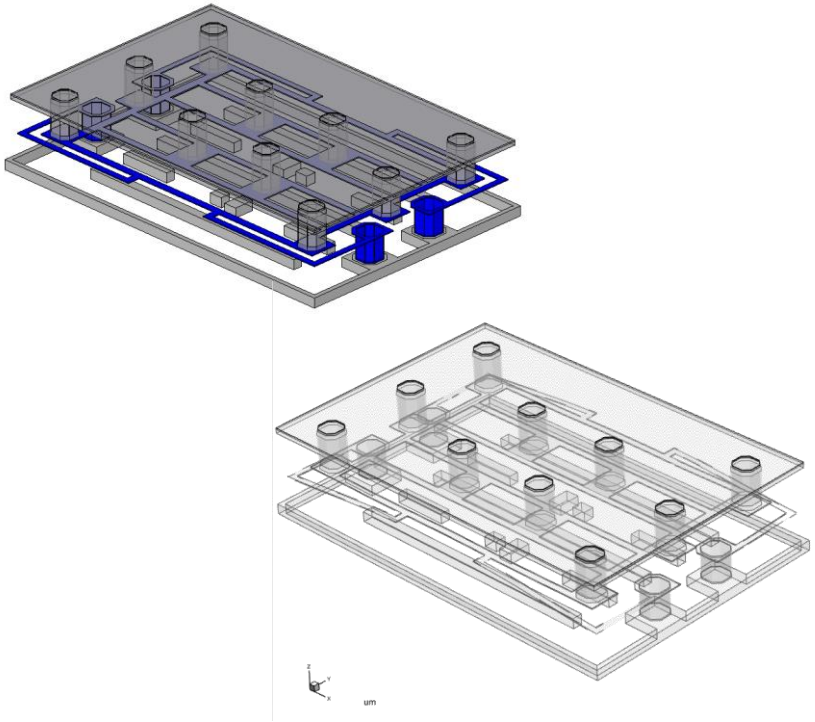
DLP Products 0.98 System Roadmap

- Provide EVM for evaluation
- Provide chip set and reference design to allow customization
- Provide controller core for system simplification

NIR Pixel Orientation

0.67 Device



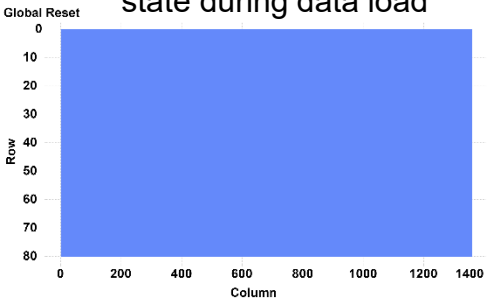


Phixel Actuation Behavior

Array Reset/Load Options

Current PLM EVM/Device

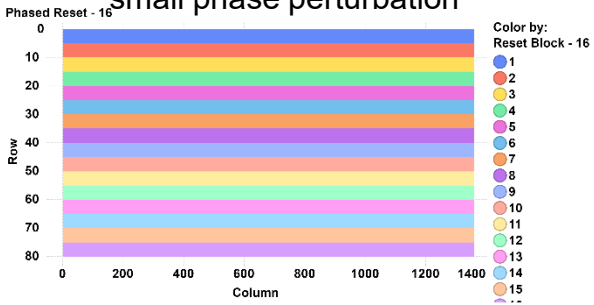
Mirrors return to undeflected state during data load



- Global load scheme
- 1 reset block, ~90us / block
- Total ~90us data load

Current PLM EVM/Device

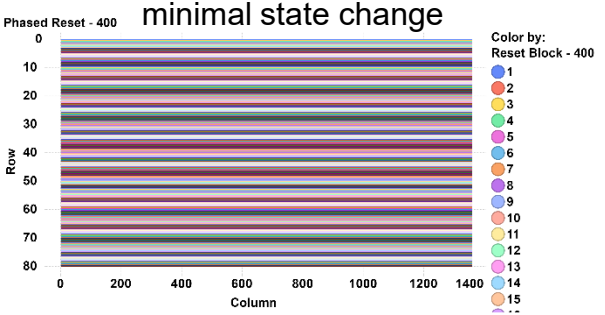
Blocks loaded sequentially, small phase perturbation



- Phased load scheme
- 16 reset blocks, ~6us / block
- Total ~90us data load time

Theoretical Future Device

Blocks loaded sequentially, minimal state change



- Phased reset scheme
- *400 reset blocks, ~0.25us / block
- Total ~90us data load time

Phased reset scheme = data loaded to blocks sequentially. See 16-block details below:

- During block 1 data load, bias is removed for ~6us.
- Depending on original state, mirrors begin transition to zero-displacement state but likely do not have enough time to return to zero-displacement state before new state (bias) is applied. Some phase perturbation expected.
- New state (bias) is applied and mirrors transition to new displacement state.

*Details TBD based on future development. Example given for potential 0.67” device.

Phixel Actuation Behavior

Global Load

- Global loading event causes all mirrors to transition to non-displaced state
- It takes ~100us to load data. Since mirrors can transition between states in ~50us, mirrors reach non-displaced states
- This interrupts/upsets the outgoing signal from the PLM

Global Operation – Mirrors return to undeflected state during data load

Phixel Actuation Behavior

Phased Load

16 Block Reset – Blocks reset sequentially, small phase perturbation

- During block 1 data load, bias is removed for ~6us
- Depending on original state, mirrors begin transition to zero-displacement state but do not have enough time to return to zero-displacement state before new state (bias) is applied.
- Some phase perturbation expected

Phixel Actuation Behavior

Fine Phased Load

~400 Block Reset – ~0.25us / block
Blocks reset sequentially,
minimal state change/phase error

*Displacement amount is for illustration purposes